REMARKS

This is a response to the Notice of Non-Compliant Amendment dated November 15, 2006 and the Final Office Action dated July 27, 2006. Claims 1-45 are pending in the application. Claims 1, 2, 5, 11, 12, 15, 23-26, 28, 34, 36 and 42-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,289, 421 to Ali et al. ("Ali") in view of U.S. Patent No. 6,678,801 to Greim et al. ("Greim"). Additionally, claims 3, 4, 6-10, 13, 14, 16-22, 27, 29-33, 35, and 37-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ali in view of Greim and further in view of U.S. Patent No. 4,744,078 to George P. Kowalczyk ("Kowalczyk"). With this response, claims 1, 11, and 24 have been amended for clarity and not for reasons relating to patentability.

With this response, the claim status identifiers have been corrected as noted in the Notice of Non-Compliant Amendment of November 15, 2006.

The rejections from the Office Action of July 27, 2006 are discussed below in connection with the various claims. No new matter has been added. Reconsideration of the application is respectfully requested in light of the following remarks.

I. REJECTIONS UNDER 35 U.S.C. § 103(a)

a. Rejections under Ali and Greim

Independent claims 1, 11, 24, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ali in view of Greim. Applicants submit that these claims, as amended, are patentable over Ali in view of Greim because the combination of these references fail to teach or suggest all of the elements of these claims. In particular, the combination of Ali and Greim fails to disclose a system that may detect a store operation by a processor "without requiring said processor to perform an act in addition to said store."

Independent claims 1, 11, 24 and 34, as amended, are set forth above.

Ali discloses, "Intelligent memory devices [that] allow for the transfer of data between two or more electronic devices, such as digital signal processors and microcontrollers." *See* Ali, Abstract. As noted in the Office Action at page 3, "Ali did not expressly detail the logic detecting when the coprocessor has stored data and to signal the processor" or vice versa. Instead, the Examiner relies on Greim.

Greim discloses, "[a] multi-processor system [which] includes a global bus (14) having associated therewith a global address space with a plurality of processor nodes (10) associated therewith." *See* Greim, Abstract. In particular, the Examiner notes that Greim discloses mailbox logic associated with a dual port memory. (Greim, col. 24, l. 48 – col. 25, l. 62.) Applicants respectfully submit that the mailbox feature disclosed in Greim is different from the claimed "control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors without requiring said processor to perform an act in addition to said store." Instead, the system of Greim requires the processor to write to a mailbox for the destination processor before an interrupt is generated. (Greim, col. 24, ll. 50-54.) These mailboxes are different than the DSPRAM memory, although they are contained within the memory. (Greim, col. 24, ll. 55-58.) Thus, the system of Greim requires the processor to store the data in the memory and also write to a mailbox, i.e. by writing a semaphore/signal separate from the store operation, associated with the destination processor, thereby alerting the control logic to the existence of the data. In contrast, Applicants claim a system that includes control logic wherein "said processor and co-processor [do] not otherwise signal[] said control logic of said store operations." Accordingly, as the claimed system signals the recipient based on the detection of a store operation of the data that is intended to be read by that recipient, separate/independent semaphores/signals generated by the sender of the data are unnecessary to signal the control logic of the presence of the data. This simplifies the design of the claimed processor and co-processor as they need not be designed to signal the control logic when they store data. Instead, the claimed control logic takes care of the necessary signaling. As neither Ali or Greim teaches the claimed control logic, their combination fails to teach the claimed control logic.

For at least these reasons, claims 1, 11, 24, and 34 are patentable over the combination of Ali and Greim.

Dependent claims 2, 5, 12, 15, 23, 25-26, 28, 36 and 42-45 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ali and Greim. Dependent claims 2, 5, 12, 15, 23, 25-26, 28, 36 and 42-45 depend, either directly or indirectly, from claims 1, 11, 24, and 34, and should be allowed for the reasons set out above for the independent claims. Applicants therefore request that the Examiner withdraw this rejection of these claims.

b. Rejections under Ali, Greim, and Kowalczyk

Dependent claims 3, 4, 6-10, 13, 14, 16-22, 27, 29-33, 35, and 37-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ali in view of Grimes and further in view of Kowalczyk. Applicants submit that these claims, as amended, are patentable over Ali in view of Greim because the combination of these references fail to teach or suggest all of the elements of these claims. In particular, the combination of Ali and Greim fails to disclose a system that may detect a store operation by a processor "without requiring said processor to perform an act in addition to said store."

As set forth above, Applicants submit that the combination of Ali and Greim fail to disclose at least control logic "operative to detect when said co-processor has stored data to said memory and to signal said processor [of the detected operation]," as claimed in claims 1, 11, 24, and 34.

Kowalczyk fails to fill the gap. Kowalczyk discloses a system in which data is transferred between a system bus (i.e. first processing entity) and a network bus (i.e. second processing entity). A microprocessor and control logic manage the data transfer. The transfer is managed using a switch that operatively connects either the system bus or the network bus to a single port of a dual ported memory. Kowalczyk, Abstract. When either the system bus or network bus wishes to transfer data, they must inform the microprocessor and control logic directly, for example, by using interrupts. See, e.g., Kowalczyk, Col. 4, lines 4-10. Accordingly, the system of Kowalczyk teaches away from control logic that detects memory store operations. As neither Gallotta et al. and Kowalczyk each fail to disclose a system that includes control logic "operative to detect when said co-processor has stored data to said memory and to signal said

processor [of the detected operation]," the combination of Gallotta et al. and Kowalczyk also fails to disclose this element of these claims.

For at least these reasons, claims 1, 11, 24, and 34 are patentable over the combination of Ali, Greim and Kowalczyk.

Dependent claims 3, 4, 6-10, 13, 14, 16-22, 27, 29-33, 35, and 37-41 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ali, Greim, and Kowalczyk. Dependent claims 3, 4, 6-10, 13, 14, 16-22, 27, 29-33, 35, and 37-41 depend, either directly or indirectly, from claim 1, 11, 24, and 34, and should be allowed for the reasons set out above for the independent claims. Applicants therefore request that the Examiner withdraw this rejection of these claims.

SUMMARY

Each of the rejections in the Notice of Non-Compliant Amendment dated November 15, 2006 and the Final Office Action dated July 27, 2006 has been addressed and no new matter has been added. Applicants submit that all of the pending claims are in condition for allowance and notice to this effect is respectfully requested. The Examiner is invited to call the undersigned if it would expedite the prosecution of this application.

Respectfully submitted,

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James L. Katz
Registration No. 42, 711
Attorney for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200